



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,699	02/02/2004	Edgar R. Zuniga-Ortiz	33535.1	8605

23494 7590 04/06/2007  
TEXAS INSTRUMENTS INCORPORATED  
P O BOX 655474, M/S 3999  
DALLAS, TX 75265

EXAMINER
----------

PHAM, HOAI V

ART UNIT	PAPER NUMBER
----------	--------------

2814

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/06/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/769,699	<b>Applicant(s)</b> ZUNIGA-ORTIZ ET AL.	
	<b>Examiner</b> Hoai v. Pham	<b>Art Unit</b> 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 1/8/2007.
- 2a) ☒ This action is **FINAL**.      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 27-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 27-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claim 31 is objected to because of the following informalities:  
  
Line 7, change "windows" to --window-- for clarifying the scope of the claim.  
  
Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 27-28 and 30-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. [U.S. Pat. 6,709,901] previously applied.

With respect to claim 31, Yamazaki et al. discloses (fig. 10B, cols. 10-11) a method for fabricating a semiconductor assembly comprising the step of:

providing a semiconductor chip (220) having a planar active surface including an integrated circuit, said integrated circuit having metallization patterns including at least one contact pad (221) at said planar active surface;

providing a protective overcoat (222) over said planar active surface, said protective overcoat including window exposing said at least one contact pad, said window having sidewalls;

providing an added conductive region (223 and 230) having at least one conductive layer (223) on said metallization pattern covering and conformal to said at least one contact pad, said sidewalls of said window and a portion of said protective overcoat surrounding said window, said added conductive layer (230) having a planar outer surface, said outer surface of said added conductive layer suitable to form metallurgical bonds without melting;

providing an assembly board (224) having at least one planar, metallurgically bondable terminal pad (225) in a distribution aligned with the distribution of said at least one contact pad (221);

aligning said added conductive region (223 and 230) and said at least one terminal pad (225) so that said at least one terminal pad (225) is connected to a corresponding terminal pad (225); and

metallurgically bonding said added conductive region (223 and 230) and said at least one terminal pad (225) without melting said outer surface of said added conductive region (223 and 230) (fig. 10b).

With respect to claims 27 and 28, Yamazaki et al. discloses that wherein said step of depositing said at least one added conductive region (230) by electroless plating (col. 11, lines 8-9).

With respect to claim 30, Yamazaki et al. (fig. 10B) discloses that wherein said step of fabricating a planar outer surface of said added conductive layer comprises the step of depositing a second of at least one added conductive layer by using the method of support by islands (222) of protective overcoat.

With respect to claim 32, Yamazaki et al. discloses that where in said bonding comprises direct welding by metallic interdiffusion (col. 11, lines 5-15).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. [U.S. Pat. 6,709,901] previously applied, in view of Akram et al. [U.S. Pat. 6,617,687] previously applied.

Yamazaki et al. substantially discloses all the limitations as claimed above. Yamazaki et al. also discloses the step of depositing said at least one added conductive layer (230) by electroless plating. Yamazaki et al. does not explicitly teach the step of depositing a second of at least one added conductive layer (230) by screen printing. However, Akram et al. discloses electroless plating, screen printing ..et. are known technique to depositing the conductive layer (66) (col. 11, lines 17-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the known technique such as screen printing as taught by, Akram et al. into the process of Yamazaki et al. to form conductive layer.

### ***Response to Arguments***

7. Applicant's arguments filed 1/8/2007 have been fully considered but they are not persuasive.

Applicant argues that the features of "an added conductive region having at least one conductive layer on said metallization pattern covering and conformal to said at least one contact pad, said sidewalls of said window and a portion of said protective overcoat surrounding said window" in claim 31 are not found in Fig. 10(b) of Yamazaki et al.

Applicant's argument are not persuasive because Yamazaki et al. clearly disclose an added conductive region (223 and 230) having at least one conductive layer (223) on said metallization pattern covering and conformal to said at least one contact pad, said sidewalls of said window and a portion of said protective overcoat surrounding said window (see fig. 10B).

### ***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

Art Unit: 2814

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



HOAI PHAM  
PRIMARY EXAMINER